

Engineering strained silicon on insulator wafers with the Smart Cut™ technology

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Abstract

Strained silicon on insulator wafers are today envisioned as a natural and powerful enhancement to standard SOI wafers and/or bulk-like strained Si layers. This paper is intended to demonstrate through miscellaneous structural results how a layer transfer technique such as the Smart Cut™ technology can be used to obtain good quality tensile-strained silicon on insulator wafers. Such a technique uses preferentially hydrogen implantation to peel-off the very top part of an epitaxial stack and transfer it onto another silicon substrate. The formation of an insulator, prior to the bonding onto a new silicon substrate enables the formation of a “semiconductor on insulator” structure. Two approaches based on the Smart Cut technique are considered in this paper. The first one relies on the formation by layer transfer of a relaxed SiGe on insulator (“SGOI”) substrate on which a tensile-strained Si layer is then grown. The second one is based on the transfer of a SiGe relaxed buffer/Si cap stack. A SiGe-free tensile-silicon on insulator (sSOI) substrate is then obtained after the selective etching of the top SiGe layer. The epitaxial layers studied in this article are of two kinds: (i) the thick, nearly fully relaxed SiGe layers (with or without tensile-strained Si layers on top depending on the final structure targeted: SGOI or sSOI) used as the donor wafers in layer transfer operations, and (ii) the thin, relaxed SiGe layers and the thin, tensile-strained Si epitaxial films grown on SGOI substrates. In-depth physical characterizations of these epitaxial layers are used to evaluate the quality of the transferred layers in terms of thickness uniformity, Ge content, strain control, dislocation densities etc... Detailed experiments are also used to demonstrate that these final substrates are compatible with future CMOS applications. The sSOI approach is particularly challenging in this respect as the strain needs to be maintained during many technological operations such as layer transfer,

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selective removal of the SiGe, high temperature thermal treatments etc. First results showing how the strain is changing during such operations are presented.

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1. Introduction

Silicon on insulator (SOI) and strained silicon have been often considered as two separate, independent and sometimes competing solutions for improving the performance of silicon based CMOS transistors. New technological solutions are being explored in order to boost circuit performance for the next logic and mixed signal generations, driven by the demands of the ITRS [1]. In particular, tensile-strained silicon is one of the most promising solutions to improve $I_{\text{on}}/I_{\text{off}}$ ratio and transconductance [2–4] when traditional device scaling faces physical limits (gate oxide tunneling, mobility reduction by high k gate dielectric, etc.). The attractiveness of strained silicon for devices is reinforced by its compatibility with CMOS integration processes, standard MOSFET architectures, and circuit layouts. The gain in mobility measured in silicon layers submitted to a biaxial tensile-strain is reported to originate from changes in the band structure and possibly also from modifications of the surface morphology [5–7]. For a moderate strain (lattice mismatch <1%) there is little gain in hole mobility. An electron mobility enhancement of up to 70% has been measured with such a strain configuration, however [8].

SOI is today the substrate of choice for high performance, low voltage, low power consumption IC applications. Tensile-strained silicon directly on insulator (“sSOI”) [9–11] combines the performance and scalability of fully depleted ultra-thin SOI and the mobility enhancement in strained silicon. For partially depleted SOI device architectures, relaxed SiGe on insulator, with a tensile-strained silicon layer on top [9,12–14], can boost circuit performance by up to 30%.

Strained silicon on SiGe epilayers on bulk Si substrates suffers from major limitations, most of them due to the use of thick, complex and defect containing buried SiGe layers (such as the well-known graded buffer layers where the Ge content is increased from 0% up to the targeted Ge concentration, typically 20%) in order to provide a template for a relaxed SiGe layer of constant Ge content [15]. This compositionally uniform layer becomes a virtual substrate for the strained Si epitaxy. Ge diffusion, strain relaxation, creation and propagation of misfit and threading dislocations, are some of the issues that limit the flexibility of CMOS integration.

Dopant diffusion indeed differs from that in Si, pn junctions suffer from a higher leakage mainly due to the smaller band gap of SiGe where the junctions are formed etc.

The present work focuses on the merger of strained silicon and SOI into engineered substrates that will enable the introduction of strained silicon on insulator (with or without a SiGe intermediary layer) wafers into mainstream microelectronics. We will first of all give some structural data on our SiGe (Si) donor wafers: (i) Ge concentration profile inside the graded layer, (ii) degree of strain relaxation and (iii) threading dislocation density of the constant composition SiGe thick layer and (iv) preservation of the tensile-strain state of the Si cap layer. Advanced transmission electron microscopy (TEM) imaging and data processing techniques have been used. We will show for the first time how photoluminescence can be used to assess the electronic quality of tensile-strained Si layers embedded in relaxed SiGe. We will then focus on the structural properties of SGOI substrates and detail, also for the first time, the specifics of the growth of SiGe and/or Si on such wafers (in terms of surface preparation, interface abruptness, surface roughness, dependence of the growth rate on the starting SiGe layer thickness etc.). Finally, we will demonstrate in TEM and in Raman spectroscopy that the tensile-strain of the Si layers of sSOI wafers is preserved during the selective etching of the SiGe layer and subsequent high temperature anneals (such as the ones that would be used to strengthen the bonding interface).

2. Smart Cut: a layer transfer technology for SOI volume production

Today, the Smart CutTM technology is used by SOITEC for mass production of SOI wafers [16,17]. Figs. 1 and 2 describe the basic steps of such a process. Atomic species (preferentially hydrogen ions) are first implanted in a donor substrate A. This step induces the formation of a quite deep weakened zone. Next, substrate A is bonded to a support B by wafer bonding. Prior to the bonding step, an insulating layer such as SiO₂ is formed at least on one of the two wafers. The splitting step that follows, which takes place inside the weakened zone, gives rise to the transfer of a thin layer

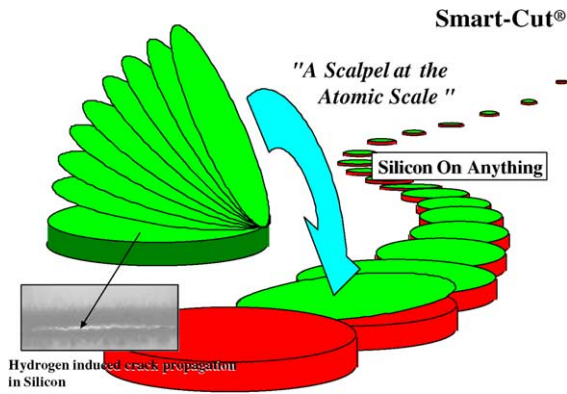


Fig. 1. Schematics of the Smart Cut technology: a scalpel at the atomic scale.

from substrate A onto the support B. Finally a treatment can be performed to remove the rough surface left after splitting. The process is well suited for the manufacturing of SOI wafers, especially for ultra-thin top silicon layers (<500 nm) with a very high silicon thickness uniformity. It also allows a large flexibility in layer thickness for the buried oxide, with values ranging from a few μm down to less than 100 nm.

3. Smart Cut engineered strained silicon on insulator: sSOI and SGOI

Fig. 3 shows an example of how a layer transfer technique such as the Smart Cut technique can be used to obtain tensile-strained silicon on insulator wafers. Here, the starting material is an epitaxial layer stack ending with relaxed SiGe on top of an intermediate graded buffer layer [15]. Using hydrogen implantation

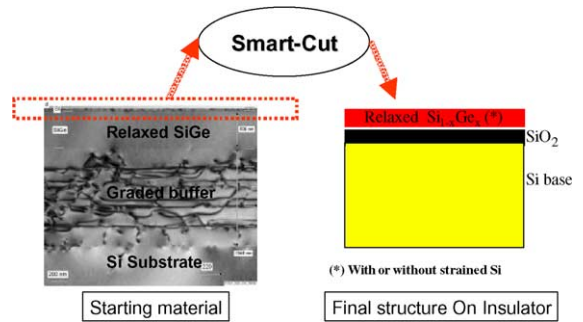


Fig. 3. Smart Cut layer transfer concept applied to the realization of SiGe on insulator and strained silicon on insulator wafers.

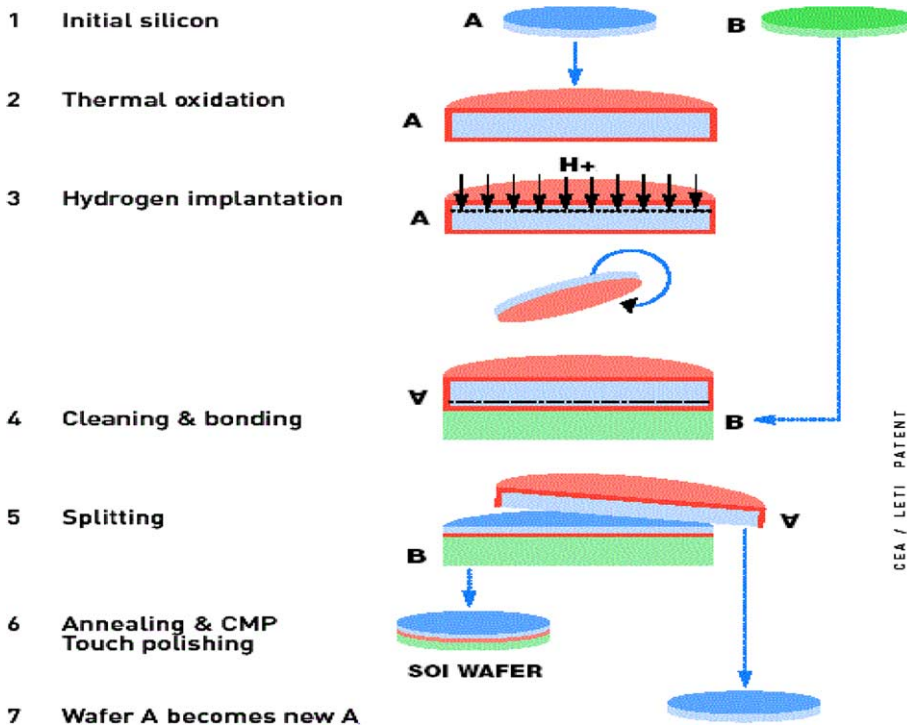


Fig. 2. Schematics of the Smart Cut technology, as used today for high volume production of SOI wafers.

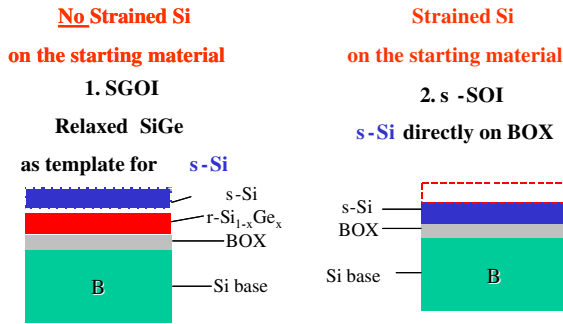


Fig. 4. Two different strained silicon on insulator structures obtained by the Smart Cut technology. In SGOI, the last step is the growth of s-Si on a relaxed SiGe layer. In sSOI, the last step is the removal by selective etching of the top relaxed SiGe film.

into the relaxed SiGe layer, the Smart Cut process is used to peel off the very top part of this epitaxial stack and transfer it onto another silicon substrate. The formation of an insulator (preferentially silicon dioxide), obtained through some thermal oxidation or oxide deposition on at least one wafer before bonding, enables the formation of a structure with a buried dielectric.

Fig. 4 illustrates schematically two approaches based on the Smart Cut technology. On the left-hand side, a few hundreds Å thick relaxed SiGe layer on insulator is formed by layer transfer; a strained Si layer is subsequently grown on top of it. In this case, known as SGOI, the total semiconductor layer thickness at the end of the process (strained Si plus relaxed SiGe) is adjusted typically in the 300–700 Å range. SGOI substrates are well adapted for partially depleted SOI architectures. On the right-hand side, the tensile-strained silicon is grown directly on the donor wafer (i.e. on the relaxed SiGe layer). A bi-layer containing the strained Si and the relaxed SiGe is then transferred by the Smart Cut process onto the handle Si substrate. After the removal of the SiGe layer (for example through a selective wet etch step [18]), the tensile-strained Si layer is exposed, forming strained silicon on insulator or sSOI. This second approach addresses the needs of fully depleted SOI architectures.

4. Structural and optical properties of the starting SiGe donor substrate

Since the final substrate is made by a layer transfer technique, the quality of the starting epitaxial stack is of prime importance. Among the critical parameters are the Ge content, the threading dislocation density, and the degree of Si strain and SiGe relaxation. For partially relaxed SiGe templates, it is necessary to go to a higher Ge content to have the same in-plane tensile-strain. The Ge concentration considered in this work is 20%. Although this is not high enough to expect any hole

mobility gain [6], the electron mobility is increased by >50%. It should be noted that the technology described here could be applied, with appropriate modifications, to achieve a Ge content that is sufficient to raise the hole mobility as well (i.e. Ge% > 35%).

The growth of a linearly graded buffer to obtain a relaxed SiGe starting layer is one of the most mature approaches to SGOI today [15]. The layer transfer technique used in this work could however be adapted (if necessary) to any other epitaxial process for growing the starting SiGe relaxed layer. As an example, one could use an epitaxial process with a thin and very defective layer to initiate the SiGe growth. Such defects may be generated, for instance, by growing a low temperature Si buffer [19]. The dislocations necessary to obtain a relaxed SiGe layer are then confined within the initial layer. Another technique is based on the growth of a strained SiGe layer on silicon and subsequent relaxation of this layer, mainly by thermal annealing. Hydrogen or helium implantation in the Si substrate underneath the SiGe layer help in confining the misfit dislocations necessary to accommodate the lattice mismatch between Si and SiGe in the implanted regions and not in the SiGe layer [20]. The starting graded buffer layers used in this project have been grown using reduced pressure-chemical vapor deposition (RP-CVD). Fig. 5 shows a typical Ge profile across the structure, with an $8\%(\mu\text{m})^{-1}$ Ge content increase in the linearly graded buffer layer. Beyond confirming good crystalline properties, XRD enabled us to check that relaxation rates were typically in the 95–98% range. Dislocation densities measured by TEM or by wet chemical revelation are typically in the $<10^6\text{ cm}^{-2}$ range.

For the sSOI approach, the strained Si layer is formed on the initial donor wafer. The determination of the misfit stress in the tensile-strained Si/relaxed SiGe

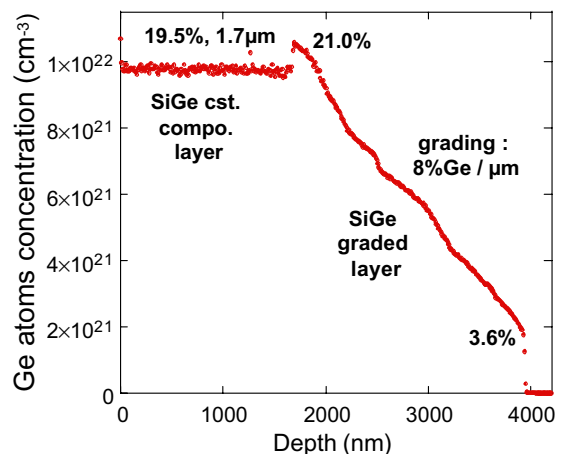


Fig. 5. SIMS depth profile of the Ge concentration inside a typical SiGe virtual substrate.

system has been performed by the Stoney curvature method [21]. This method is based on the measurement of the curvature induced by the natural elastic relaxation of the misfit stress. A simple relation exists between this misfit stress, the radius of curvature R , the thicknesses of the epitaxial layer t_l and of the substrate t_s [22]. Plan-view samples of an overall thickness of about 300–500 nm including a very thin (<20 nm) pseudomorphic top layer are particularly well adapted for such measurements. The uniformity of the misfit stress and the absence of dislocations (no plastic relaxation) is easily checked by observing the displacement and contrast of the bend contours while tilting the specimen. The overall thickness of the specimen is measured by using the variation of the diffracted intensity I_{220} as a function of the Bragg error [22]. The radius of curvature is directly determined from the bright field image shown in Fig. 6 by measuring the distance D_0 between the 440 bend contours. In the image shown, $R = 40D_0$. Curvature radii larger than 100 μm can be measured by this method.

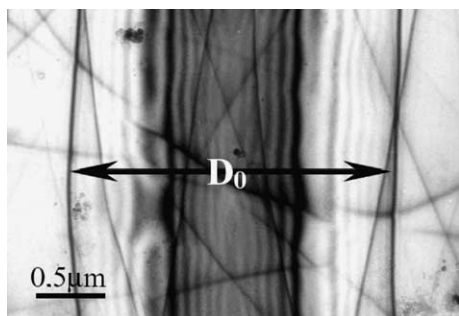


Fig. 6. Bright field image showing the 440 bend contours used for measuring a curvature radius: here, for $D_0 = 2 \mu\text{m}$, $R = 80 \mu\text{m}$.

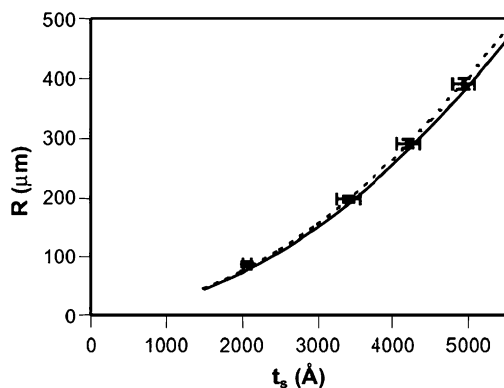


Fig. 7. Curvature radius versus substrate thickness: comparison between experiments and best fit obtained for $\sigma = 1.35 \text{ GPa}$.

Experimental (R, t_s) values were measured and are shown in Fig. 7. The misfit stress in the Si layer is the adjustable parameter allowing the best fit between the theory and experiment. Here the best fit is obtained for a misfit stress of $1.35 \pm 0.2 \text{ GPa}$, which is in good agreement with the theoretical value expected for a lattice mismatch of 0.76% due to a Ge concentration of 20%.

High resolution TEM (HRTEM) experiments performed on cross-sectional samples can also be used to measure the deformation of strained Si layers grown on SiGe. With such a technique, the displacements in the direction perpendicular to the surface can be probed. Fig. 8 is an HRTEM image taken along the $[110]$ zone axis. The $\{1-11\}$ and $\{-111\}$ planes continuously cross the Si/SiGe interface and no dislocations are found. The displacements of the Si-(002) planes relative to the SiGe-(002) planes can be quantitatively measured using the “geometrical phase method” developed by Hÿtch et al. [23]. For this, the displacement shifts of the two sets of (111) planes in Si are measured with respect to their position in SiGe. By combining these displacements, the relative shift of the Si(002) planes as a function of the distance from the Si/SiGe interface can be extracted. The results are reported in the diagram below the HRTEM image in Fig. 8. The linear decay of

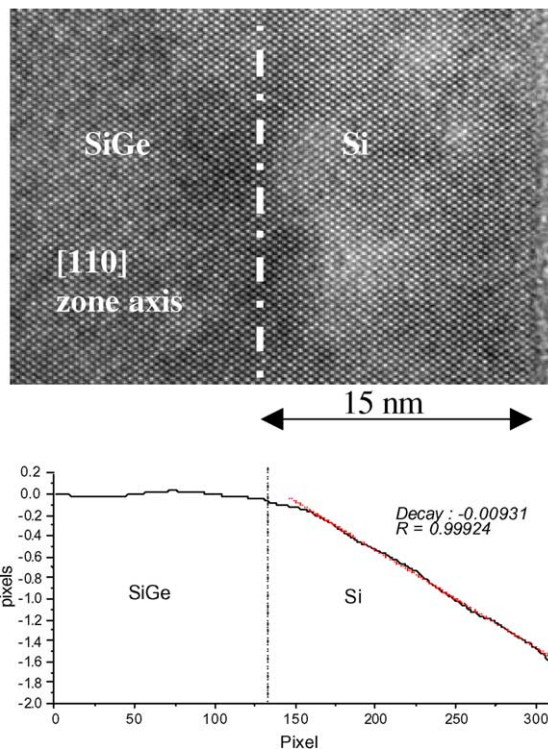


Fig. 8. (Top) Cross-sectional high resolution TEM micrograph of a 15 nm thick Si layer epitaxially grown on SiGe and studied along the $[110]$ zone axis. (Bottom) Displacements of the (002) planes in Si relative to their position in SiGe.

the (002) planes displacement in the strained Si layer is a proof of the strain homogeneity in the direction perpendicular to the surface. The perpendicular relative strain ($\alpha = \frac{d_{(002)\text{Si}} - d_{(002)\text{SiGe}}}{d_{(002)\text{SiGe}}}$) is given by the derivative of this displacement function (here, the slope of the straight line). From Fig. 4, we obtain $\alpha = -0.93\%$. In principle, ϵ_{zz} the strain component in the perpendicular direction in Si can be deduced from the exact value of the cell parameter of the SiGe material taken as reference, $\epsilon_{zz} = (\alpha - f) \frac{a_{\text{Si}}}{a_{\text{SiGe}}}$ where “ f ” is the misfit between Si and SiGe. However, results from this technique have to be taken with some caution, since the biaxial stress measured on the very thin foils examined by HRTEM can be significantly different from the one present in wafers due to possible surface relaxation mechanisms.

The tensile-strained silicon layers grown on relaxed SiGe buffer layers have also been characterized by low temperature photoluminescence. At low excitation densities, the photoluminescence is dominated by the radiative recombination associated with the dislocations in the buffer layer along with the no-phonon and phonon-assisted band-edge luminescence of the relaxed SiGe buffer layer. The photoluminescence of a strained silicon quantum well can be observed at high excitation densities [24]. Fig. 9 shows a characteristic low temperature photoluminescence spectrum of a 12 nm thick strained Si quantum well embedded in a relaxed $\text{Si}_{0.8}\text{Ge}_{0.2}$ layer. The low energy resonances at 804, 854 and 924 meV correspond to the D1, D2 and D4 recombination in the graded buffer layer respectively. The resonant lines at 960 and 1018 meV correspond to the phonon-assisted and to the no-phonon recombination in the tensile-strained Si quantum well. These emission lines correspond to a type II radiative recombination between electrons confined in the Si layer and holes trapped at

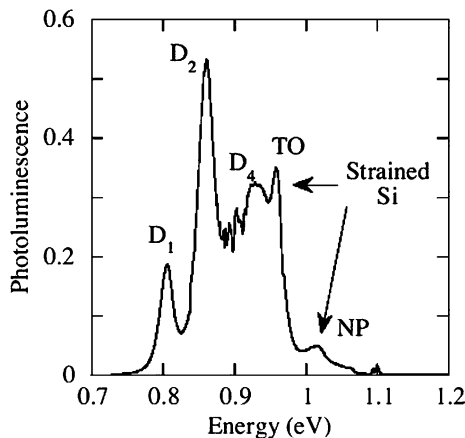


Fig. 9. Low temperature (5 K) photoluminescence of a heterostructure containing a strained Si quantum well embedded in a relaxed $\text{Si}_{0.8}\text{Ge}_{0.2}$ buffer layer. The excitation density delivered by an argon ion laser is 20 W cm^{-2} .

the hetero-interface between Si and SiGe. The energy of the recombination is in agreement with the calculated energy, which accounts for the charge distribution of the carriers in the multilayer structure. The observation of radiative recombination in the strained silicon is a signature of the high optical quality of the as-grown samples, measured before transfer to the handle substrate.

5. The SiGe on insulator substrates

Fig. 10 shows as an illustration a 200 mm SiGe on insulator wafer. A transfer of the SGOI process to 300 mm should be straightforward. Fig. 11 shows a TEM cross-section image of a SGOI substrate ready for final strained Si epitaxy. Notice the sharpness of the interfaces. Based only on this viewgraph, one can conclude that the threading dislocation density is below 10^7 cm^{-2} .

In order to accurately measure crystal defect densities, we have used plan-view TEM but also a Chemical Preferential Etching technique (see [25] for general information) developed for the characterization of thin SiGe films (<100 nm). The SiGeOI sample surface after chemical treatment can be seen in Fig. 12. A threading



Fig. 10. A 200 mm relaxed SiGe on insulator substrate.



Fig. 11. Cross-sectional TEM image of a SiGe on insulator wafer (ready for strained Si epitaxial re-growth).

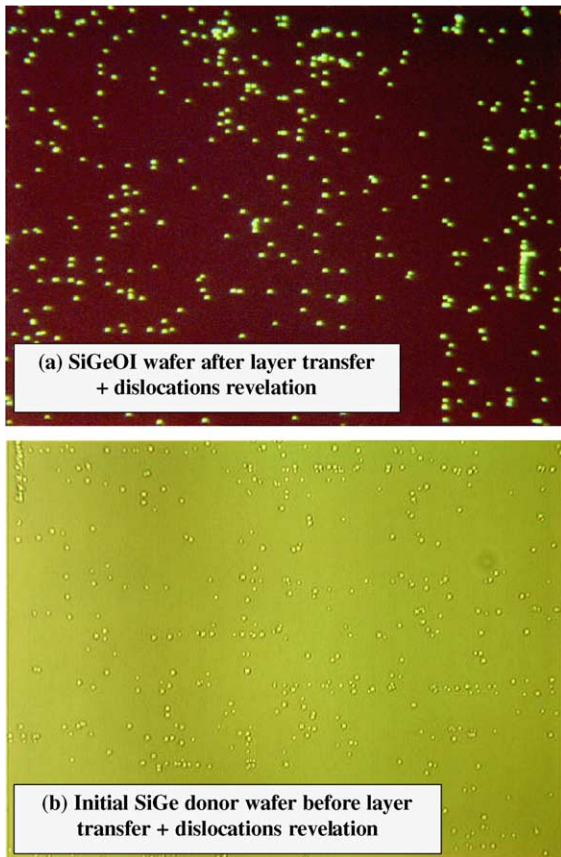


Fig. 12. Optical microscopy surface image after a chemical preferential etching treatment of (a) a SiGeOI substrate (after layer transfer) and (b) a SiGe initial donor wafer (before layer transfer). The image dimensions are $240\ \mu\text{m} \times 180\ \mu\text{m}$. The edges are aligned along the $\langle 110 \rangle$ crystallographic directions.

dislocation density of $7\text{--}8 \times 10^5\ \text{cm}^{-2}$ is measured from Fig. 12a. This value is similar to the one associated with bulk SiGe donor substrates before layer transfer (Fig. 12b). This result confirms that the layer transfer process does not introduce additional dislocations. Further improvements in terms of dislocations densities at the SiGeOI level therefore rely on the starting donor wafers.

Initial SiGe layer transfer focused on $>100\ \text{nm}$ thick layers to study the mechanical properties of the transferred film and resulting composite substrate. Ultra-thin SGOI with SiGe thicknesses ranging from 60 down to 10 nm have been also investigated. The impact of such a thickness on the strained Si epitaxial growth will be addressed in the next section.

6. Epitaxial growth on SGOI substrates

The SGOI substrates are used as templates for the growth of tensile-strained Si layers. This epitaxial step is

very sensitive to the transferred SiGe film quality. Before addressing strained Si epitaxy on ultra-thin SGOI, 100 nm relaxed SiGe layers were grown on SGOI to better assess the quality of the SiGe transferred layer. The main purpose was to enlarge crystalline defects that might be present near the surface. Homoepitaxy is also interesting in that it does not introduce any additional parameters that could interfere in the characterization of the transferred SiGe film.

As in the case of the starting material, the silicon and SiGe epitaxy have been performed on blank wafers by means of RP-CVD. The deposition pressure was set to 20 Torr. The carrier gas was hydrogen; its flow was maintained constant at a few tens of standard liters per minute. The process gases were dichlorosilane (SiH_2Cl_2) and germane (GeH_4). Such gases will enable us in the next phase of the project to achieve if necessary selective deposition inside Si windows of dielectric-masked wafers.

The surface preparation prior to deposition is a standard HF-last wet cleaning. It consists of a diluted HF dip, followed by a rinse in a de-oxygenated and de-ionized water, with final drying in isopropyl alcohol vapors. Such a sequence allows us to remove the native oxide, and have the dangling bonds tied by hydrogen or fluorine atoms to protect the wafer surface during its transfer from the wet cleaning bench to the RP-CVD load-lock. An in situ H_2 bake at $850\ ^\circ\text{C}$ for 2 min is then carried out on our SGOI substrates in order to remove the remaining traces of oxide and other surface contaminants. After wet cleaning and in situ H_2 bake, epitaxial surfaces are suitable for strained silicon growth. Carbon and oxygen content is very low, as shown in Fig. 13. Surface roughness (AFM $1\ \mu\text{m} \times 1\ \mu\text{m}$ scans) is typically 0.2 nm rms, and the z range = 1.7 nm [26]. An even better surface roughness has been recently obtained: 0.15 nm rms and a z range of 1.4 nm, respectively. For reference, surface roughness measured on bulk polished Si wafers or SOI wafers are typically in the 0.1 nm rms range.

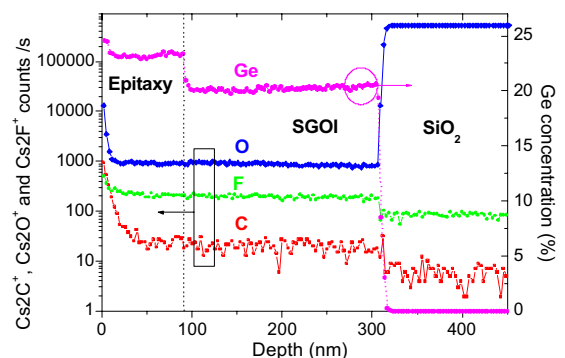


Fig. 13. SIMS depth profiles of the Ge concentration (right scale) and of some typical contaminants (left scale).

6.1. Thick SiGe film growth

The thickness of the SiGe layer grown onto our SGOI substrate was nominally 100 nm; the germanium concentration was set to be the same as in the transferred SiGe film (i.e. 20%). The same deposition parameters in terms of mass flows, temperature (750 °C) etc. were indeed used to form the constant composition SiGe layer of the donor wafer. The resulting SiGe epitaxial film is smooth. No pits are observed. AFM measurements reveal that the surface developed a slight cross-hatch pattern after epigrowth. The cross-hatch appearance (not present before epitaxy) is not linked to a dramatic roughness increase of the surface. The rms roughness was 0.2 nm, the z range 2.3 nm. Those values are similar to the ones prior to epitaxy.

In Fig. 13, we have plotted the C, O, F (usual contaminants) and Ge SIMS depth profiles. The film grown has a larger germanium concentration (23% instead of 20%) than the template, even though the two films were grown using the same process parameters. The deposited thickness was also slightly less than the one expected (92 instead of 100 nm). Those two observations most probably mean that the real surface temperature of the SGOI substrate is lower than the one of SiGe donor substrates, in spite of the same nominal growth temperature. Same effects seem to happen when thin strained Si is grown onto SGOI (see next section). No C, O or F contaminant peaks can be observed at the interface between the two SiGe films, validating the surface preparation used.

The XRD omega–2 theta scan displayed in Fig. 14 shows that both the initial transferred SiGe layer and the epitaxial film grown on top of it have a good crystalline quality. Indeed, the layer peaks are well defined and intense. The presence of two peaks is due to the fact that

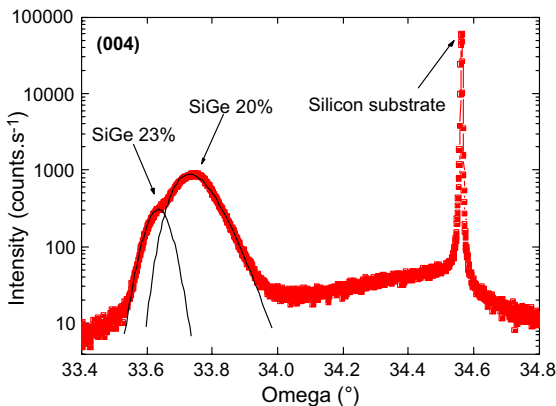


Fig. 14. Omega–2 theta XRD scan around the (004) Si diffraction order in high resolution X-ray diffraction for the {SiGe epilayer/SGOI} stack of Fig. 13.

the Ge concentration is not the same in the epitaxial layer and in the SiGeOI template underneath. The angular positions of the SiGe peaks with respect to the Si substrate do not enable one to determine the Ge concentration of the layer. They are indeed at too low diffraction angles for such Ge concentrations. The most likely explanation might be a tilt between the silicon substrate and the transferred SiGe film as can be expected during a layer transfer involving wafer bonding (wafer to wafer misalignment concerning twist and tilt).

6.2. Thin strained Si growth

Tensile-strained Si was also directly grown at 700 °C onto SGOI substrates (targeted Si thickness: 15 nm). AFM scans showed no re-appearance of the cross-hatch pattern. The surface rms roughness was 0.3 nm and the z range 2.8 nm, which is similar to the surface roughness of the initial surface prior to epitaxy. SIMS and XRD could not be used since the strained Si film is too thin. The deposited silicon thickness (measured mainly by spectroscopic ellipsometry, but also in TEM) increases as the initial thickness of the SiGe transferred film decreases, as illustrated in Fig. 15. The same phenomena was obtained for tensile-strained silicon epitaxy carried out on mesa isolated SiGeOI wafers. In order to make sure that this effect was not an artifact due to thickness measurement by spectroscopic ellipsometry (SE), TEM has also been used. TEM results (see Fig. 15), although not perfectly aligned with SE results, confirm the trend. Variations in surface emissivity (and thus growth temperature) as the SiGe layer thickness changes might explain such a behavior. Such a behavior has already been observed on ultra-thin conventional SOI wafers on which a Si layer has been epitaxially grown [27]. In this case, as the growth temperature was larger on thinner

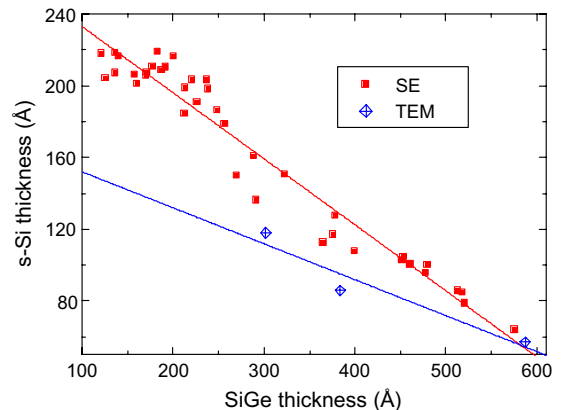


Fig. 15. Evolution in SE and in TEM (same sample) of the strained silicon thickness deposited (for a given deposition time) as a function of the starting SiGe on oxide thickness.

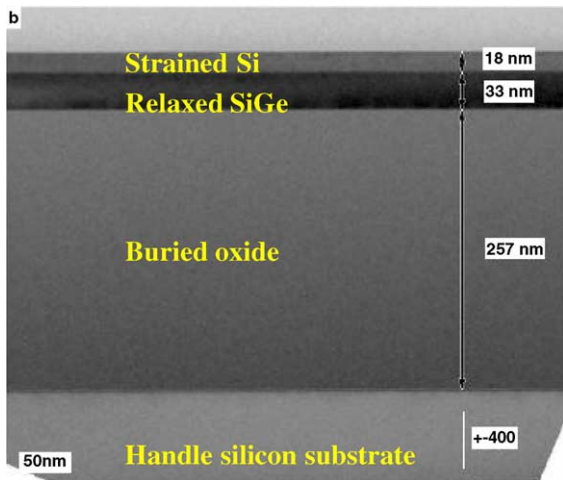


Fig. 16. Cross-sectional TEM picture showing 18 nm thick strained Si grown onto a 33 nm thick SGOI substrate (sample different from the one of Fig. 15).

parts of the SOI layers, the net result was an improvement during epitaxy of the total Si thickness uniformity.

The final structures, after strained Si epitaxial growth, have also been characterized by cross-sectional TEM. An example corresponding to a 18 nm thick strained Si layer grown on top of a 33 nm thick SiGeOI substrate is shown in Fig. 16. Again in this case, no threading dislocations can be observed, and the Si/SiGe interface is quite sharp.

7. The sSOI substrates

For this approach, the final structure is SiGe free. Since the initial layer that enabled to build the strain Si is eventually suppressed, the wafer bonding interface has to maintain it through the following steps. This point is certainly the most ambitious challenge that needed to be checked when such a process was envisioned. The results reported here have been obtained with standard bonding conditions, appropriate for SOI wafers realization for the Smart Cut process. We will see that the results that have been obtained here in terms of strain relaxation do not show any requirement for the use of specific high energy wafer bonding preparations.

After the SiGe/tensile-strained Si bi-layer transfer, the SiGe film was selectively removed by wet etching (Fig. 17). The crystalline quality and the residual strain inside the Si layers were investigated by TEM and Raman spectroscopy. The TEM curvature method cannot be used as described in Section 4 because of the strained Si/oxide/substrate structure. However, in plan-view geometry and for SiO₂ layers <300 nm, electrons can be diffracted in both the Si substrate and in the thin

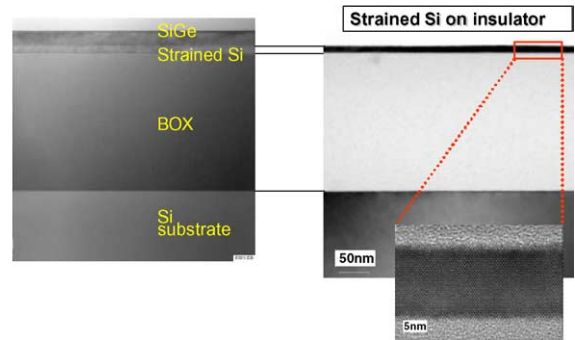


Fig. 17. Cross-sectional TEM pictures of 200 mm relaxed SiGe on insulator wafers, before and after the removal of the SiGe over-layer (then generating a sSOI substrate).

Si layer resulting in double diffraction. Images formed using such double diffracted beams show 2D moiré patterns, which are characteristic of the small differences in inter-planar spacing of the two decoupled lattices. An example of such an image is shown in Fig. 18. The uniformity of spacing and the direction of the moiré fringes are proofs of the strain uniformity in the plane parallel to the surface of the wafer. From the measurement of the relative disorientation of the two layers and of the moiré spacing [28], one can easily deduce the “in plane” strain and thus the stress in the top Si layer. A value in the 1.2–1.3 GPa range was found using Fig. 18 image. This value is close (see Fig. 6) to what would be

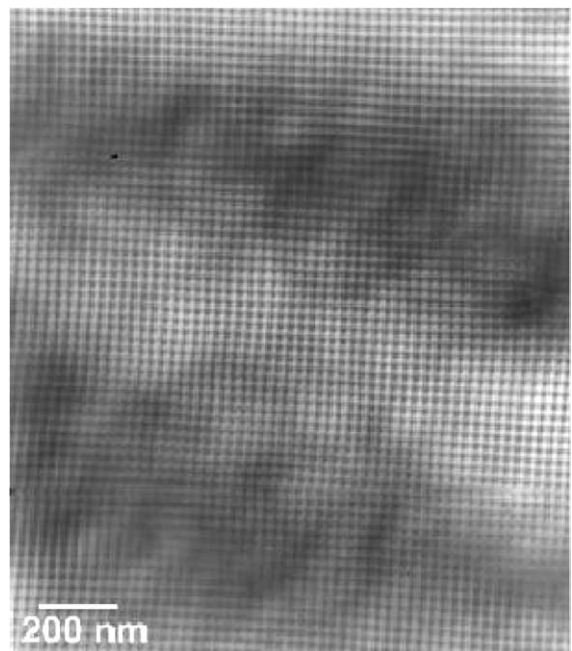


Fig. 18. Plan-view bright field $\langle 001 \rangle$ image of a 15 nm Si layer transferred onto SiO₂.

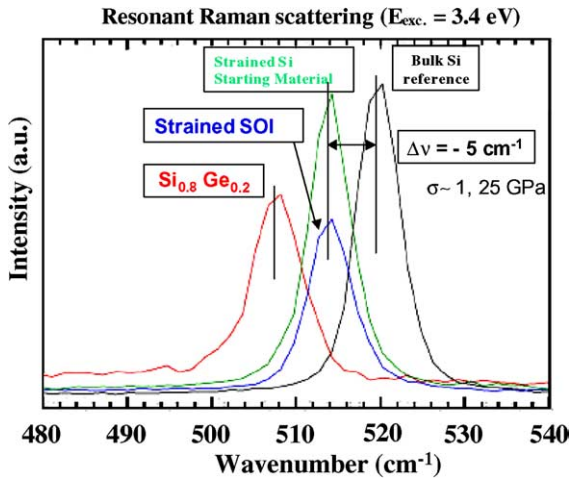


Fig. 19. UV-Raman spectra showing that the tensile-strain inside the Si layer is maintained throughout the Smart Cut transfer and the SiGe over-layer removal.

expected for a Si layer in a tensile-strain configuration on relaxed Si_{0.8}Ge_{0.2}. From these TEM observations it can be concluded that there is no significant stress relaxation during the layer transfer process, the SiGe layer removal step and thermal treatments.

Fig. 19 shows the Raman spectra of the strained silicon layer/SiGe donor substrate and of the strained Si after the total removal of the SiGe layer. It can be seen that the tensile-strain is maintained, confirming the TEM results.

The sSOI approach raises in particular a question about the stability of the strain during CMOS processing because the relaxed SiGe reference lattice has been removed. In order to partially answer this question high temperature thermal treatments have been simulated. Although rapid thermal annealing will be mainly used in advanced CMOS manufacturing, the worst-case scenario of furnace anneals was tested, for duration of 15 and 30 min. Fig. 20 shows the evolution of the strain as measured by UV Raman when the sSOI samples are annealed under different conditions (15 and 30 min, different atmospheres, ...). No significant strain relaxation is observed from such measurements. Fig. 21 focuses on the effects of the annealing temperature (from 800 up to 1000 °C) when all other parameters are fixed. In this case, the duration is fixed at 15 min. One can see that the Raman peak position does not go back to higher values (which would mean some plastic strain relaxation) but instead is quite constant. Up to 900 °C, no shift at all can be detected while beyond 900 °C a very slight shift seems to appear. The latter however is in the opposite direction (even further away from the bulk relaxed silicon) that one could expect from some partial relaxation. Further studies and characterizations are under way to understand this effect.

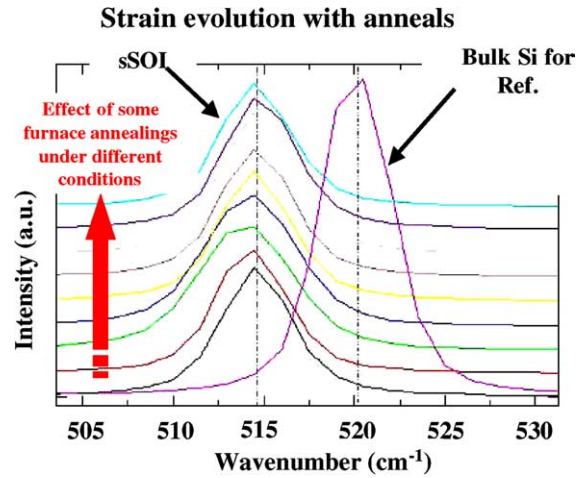


Fig. 20. UV-Raman spectra showing that the tensile-strain inside the Si layer is maintained during different thermal treatments at temperatures up to 1000 °C for 15 min.

UV Raman sSOI strain evolution as a function of the annealing temperature (15 minutes anneals)

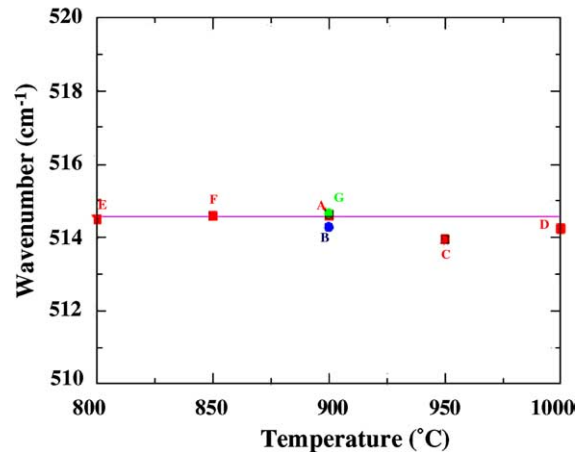


Fig. 21. UV-Raman spectra showing the strain evolution inside the s-Si layer for different thermal treatments at temperatures up to 1000 °C for 15 min.

8. Conclusions

Tensile-strained silicon on insulator wafers are today envisioned as a natural and powerful alternative to standard SOI and/or bulk-like strained Si layers. We have shown two examples of how a layer transfer technique such as the Smart Cut process can advantageously be applied to the realization of tensile-strained silicon on insulator or SiGe on insulator structures.

One approach based on Smart Cut uses a layer transfer to form an intermediate relaxed SiGe on insulator (SGOI) substrate on which the final strained Si

epitaxial growth is performed. The other approach is based on the transfer of a preformed strained Si layer. In this case, a SiGe-free substrate can be realized, which is particularly attractive for the transistor realization. However here, the tensile-strain inside the Si layer needs to be maintained during many CMOS technological operations such as layer transfer, selective removal of the SiGe layer and high temperature thermal treatments. Results shown in this study indicate that sSOI offers a process window large enough for the Smart Cut technology to be used and for subsequent CMOS integration.

Detailed experiments and characterization were performed to show that SGOI and sSOI substrates are compatible with the most advanced applications. The effects of high temperature treatments, the surface quality and interface abruptness, the Ge content and strain control have been investigated quite in-depth. The re-epitaxy of relaxed SiGe and strained Si layers has been discussed in details as well.

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